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**PALM INTRANET**

## Inventor Information for 10/619821

Inventor Name	City	State/Country
CHO, GEUN-HEE	KYUNGKI-DO	KOREA, REPUBLIC OF
KIM, KYU-HYOUN	KYUNGKI-DO	KOREA, REPUBLIC OF

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**PALM INTRANET****Inventor Name Search Result**

Your Search was:

Last Name = CHO

First Name = GEUN-HEE

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<a href="#">09559265</a>	<a href="#">6236619</a>	150	04/27/2000	Synchronous dynamic random access memory semiconductor device having write-interrupt-write function	CHO, GEUN-HEE
<a href="#">10619821</a>	Not Issued	30	07/14/2003	Delay locked loop circuit for internally correcting duty cycle and duty cycle correction method thereof	CHO, GEUN-HEE
<a href="#">10716146</a>	Not Issued	41	11/18/2003	Time delay compensation circuit comprising delay cells having various unit time delays	CHO, GEUN-HEE
<a href="#">10970016</a>	Not Issued	41	10/22/2004	Data output driver that controls slew rate of output signal according to bit organization	CHO, GEUN-HEE
<a href="#">11005821</a>	Not Issued	71	12/07/2004	Duty cycle correction circuits suitable for use in delay-locked loops and methods of correcting duty cycles of periodic signals	CHO, GEUN-HEE

**Inventor Search Completed: No Records to Display.**

**Search Another: Inventor**

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<input type="text" value="CHO"/>	<input type="text" value="GEUN-HEE"/>	<input type="button" value="Search"/>

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## Inventor Name Search Result

Your Search was:

Last Name = KIM

First Name = KYU-HYOUN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
<u>09521904</u>	6327190	150	03/09/2000	Complementary differential input buffer for a semiconductor memory device	KIM, KYU-HYOUN
<u>09525730</u>	Not Issued	161	03/14/2000	Input circuit having voltage generator shared by multiple input buffers	KIM, KYU-HYOUN
<u>09685266</u>	6414517	150	10/10/2000	INPUT BUFFER CIRCUITS WITH INPUT SIGNAL BOOST CAPABILITY AND METHODS OF OPERATION THEREOF	KIM, KYU-HYOUN
<u>09713968</u>	6366148	150	11/16/2000	Delay locked loop circuit and method for generating internal clock signal	KIM, KYU-HYOUN
<u>09718158</u>	6359481	150	11/22/2000	Data synchronization circuit	KIM, KYU-HYOUN
<u>09808024</u>	6388485	150	03/15/2001	DELAY-LOCKED LOOP CIRCUIT HAVING MASTER-SLAVE STRUCTURE	KIM, KYU-HYOUN
<u>09816968</u>	6452432	150	03/23/2001	SIGNAL PROCESSING CIRCUITS HAVING A PAIR OF DELAY LOCKED LOOP (DLL) CIRCUITS FOR ADJUSTING A DUTY-CYCLE OF A PERIODIC DIGITAL SIGNAL AND METHODS OF OPERATING SAME	KIM, KYU-HYOUN
<u>09826566</u>	6466071	150	04/05/2001	METHODS AND CIRCUITS FOR CORRECTING A DUTY-CYCLE OF A SIGNAL	KIM, KYU-HYOUN
<u>09850019</u>	6459314	150	05/07/2001	DELAY LOCKED LOOP CIRCUIT HAVING DUTY CYCLE CORRECTION FUNCTION AND DELAY LOCKING METHOD	KIM, KYU-HYOUN

<u>09861954</u>	<u>6535051</u>	150	05/21/2001	CHARGE PUMP CIRCUIT	KIM, KYU-HYOUN
<u>09875364</u>	<u>7085336</u>	150	06/05/2001	SIGNAL TRANSMISSION CIRCUIT AND METHOD FOR EQUALIZING DISPARATE DELAY TIMES DYNAMICALLY, AND DATA LATCH CIRCUIT OF SEMICONDUCTOR DEVICE IMPLEMENTING THE SAME	KIM, KYU-HYOUN
<u>09935096</u>	<u>6486719</u>	150	08/22/2001	FLIP-FLOP CIRCUITS HAVING DIGITAL-TO-TIME CONVERSION LATCHES THEREIN	KIM, KYU-HYOUN
<u>10101475</u>	<u>6590421</u>	150	03/19/2002	SEMICONDUCTOR DEVICE AND METHOD OF OUTPUTTING DATA THEREIN	KIM, KYU-HYOUN
<u>10108671</u>	<u>6693842</u>	150	03/28/2002	SEMICONDUCTOR DEVICE HAVING A PLURALITY OF OUTPUT SIGNALS	KIM, KYU-HYOUN
<u>10112108</u>	<u>6639868</u>	150	03/28/2002	SDRAM HAVING DATA LATCH CIRCUIT FOR OUTPUTTING INPUT DATA IN SYNCHRONIZATION WITH A PLURALITY OF CONTROL SIGNALS	KIM, KYU-HYOUN
<u>10160703</u>	<u>6704228</u>	150	05/30/2002	SEMICONDUCTOR MEMORY DEVICE POST-REPAIR CIRCUIT AND METHOD	KIM, KYU-HYOUN
<u>10191413</u>	<u>6590434</u>	150	07/10/2002	DELAY TIME CONTROLLING CIRCUIT AND METHOD FOR CONTROLLING DELAY TIME	KIM, KYU-HYOUN
<u>10340831</u>	<u>6734707</u>	150	01/13/2003	DATA INPUT CIRCUIT FOR REDUCING LOADING DIFFERENCE BETWEEN FETCH SIGNAL AND MULTIPLE DATA IN SEMICONDUCTOR DEVICE	KIM, KYU-HYOUN
<u>10405484</u>	<u>6853317</u>	150	04/03/2003	CIRCUIT AND METHOD FOR GENERATING MODE REGISTER SET CODE	KIM, KYU-HYOUN
<u>10611255</u>	<u>6847559</u>	150	07/01/2003	INPUT BUFFER CIRCUIT OF A SYNCHRONOUS SEMICONDUCTOR MEMORY DEVICE	KIM, KYU-HYOUN
<u>10619821</u>	Not	30	07/14/2003	Delay locked loop circuit for	KIM, KYU-

	Issued			internally correcting duty cycle and duty cycle correction method thereof	HYOUN
<u>10631412</u>	<u>7035148</u>	150	07/30/2003	OUTPUT DRIVER CAPABLE OF CONTROLLING SLEW RATE OF OUTPUT SIGNAL ACCORDING TO OPERATING FREQUENCY INFORMATION OR CAS LATENCY INFORMATION	KIM, KYU-HYOUN
<u>10631414</u>	<u>6870776</u>	150	07/30/2003	DATA OUTPUT CIRCUIT IN COMBINED SDR/DDR SEMICONDUCTOR MEMORY DEVICE	KIM, KYU-HYOUN
<u>10645018</u>	<u>6954094</u>	150	08/21/2003	SEMICONDUCTOR MEMORY DEVICE HAVING PARTIALLY CONTROLLED DELAY LOCKED LOOP	KIM, KYU-HYOUN
<u>10656303</u>	<u>6934215</u>	150	09/04/2003	SEMICONDUCTOR MEMORY DEVICE HAVING DUTY CYCLE CORRECTION CIRCUIT AND INTERPOLATION CIRCUIT INTERPOLATING CLOCK SIGNAL IN THE SEMICONDUCTOR MEMORY DEVICE	KIM, KYU-HYOUN
<u>10671105</u>	<u>6980036</u>	150	09/25/2003	SEMICONDUCTOR DEVICE COMPRISING FREQUENCY MULTIPLIER OF EXTERNAL CLOCK AND OUTPUT BUFFER OF TEST DATA AND SEMICONDUCTOR TEST METHOD	KIM, KYU-HYOUN
<u>10672461</u>	<u>6999375</u>	150	09/26/2003	SYNCHRONOUS SEMICONDUCTOR DEVICE AND METHOD OF PREVENTING COUPLING BETWEEN DATA BUSES	KIM, KYU-HYOUN
<u>10716146</u>	Not Issued	41	11/18/2003	Time delay compensation circuit comprising delay cells having various unit time delays	KIM, KYU-HYOUN
<u>10774933</u>	<u>7057433</u>	150	02/09/2004	DELAY-LOCKED LOOP (DLL) CAPABLE OF DIRECTLY RECEIVING EXTERNAL CLOCK SIGNALS	KIM, KYU-HYOUN
<u>10793001</u>	<u>7015739</u>	150	03/04/2004	INTEGRATED CIRCUIT DEVICES HAVING DUTY	KIM, KYU-HYOUN

				CYCLE CORRECTION CIRCUITS THAT RECEIVE CONTROL SIGNALS OVER FIRST AND SECOND SEPARATE PATHS AND METHODS OF OPERATING THE SAME	
<u>10793209</u>	<u>7038972</u>	150	03/04/2004	DOUBLE DATA RATE SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY SEMICONDUCTOR DEVICE	KIM, KYU- HYOUN
<u>10799783</u>	Not Issued	41	03/12/2004	Internal voltage generating circuit for semiconductor device	KIM, KYU- HYOUN
<u>10837391</u>	Not Issued	30	04/29/2004	Spread spectrum clock generator	KIM, KYU- HYOUN
<u>10841866</u>	Not Issued	93	05/06/2004	HYPER-RING OSCILLATOR	KIM, KYU- HYOUN
<u>10884723</u>	<u>7123520</u>	150	07/02/2004	BUFFER CIRCUIT AND MEMORY SYSTEM FOR SELECTIVELY OUTPUTTING DATA STROBE SIGNAL ACCORDING TO NUMBER OF DATA BITS	KIM, KYU- HYOUN
<u>10890493</u>	Not Issued	71	07/13/2004	Interface circuit and signal clamping circuit using level-down shifter	KIM, KYU- HYOUN
<u>10925522</u>	Not Issued	61	08/25/2004	Jitter suppressing delay locked loop circuits and related methods	KIM, KYU- HYOUN
<u>10949165</u>	<u>7091741</u>	150	09/24/2004	INPUT BUFFER CAPABLE OF REDUCING INPUT CAPACITANCE SEEN BY INPUT SIGNAL	KIM, KYU- HYOUN
<u>10990412</u>	Not Issued	71	11/18/2004	Input buffer for detecting an input signal	KIM, KYU- HYOUN
<u>11005821</u>	Not Issued	71	12/07/2004	Duty cycle correction circuits suitable for use in delay-locked loops and methods of correcting duty cycles of periodic signals	KIM, KYU- HYOUN
<u>11154725</u>	Not Issued	30	06/15/2005	Level shifting circuit and method reducing leakage current	KIM, KYU- HYOUN
<u>11158013</u>	Not Issued	41	06/21/2005	Delay locked loops and methods using ring oscillators	KIM, KYU- HYOUN
<u>11176396</u>	Not Issued	30	07/08/2005	Output driver and method thereof	KIM, KYU- HYOUN
<u>11220180</u>	Not	30	09/06/2005	Sense amplifier with low common	KIM, KYU-

	Issued			mode differential input signal	HYOUN
<a href="#">11243369</a>	Not Issued	25	10/04/2005	Semiconductor driver circuit with signal swing balance and enhanced testing	KIM, KYU-HYOUN
<a href="#">11258565</a>	Not Issued	30	10/25/2005	Semiconductor memory device	KIM, KYU-HYOUN
<a href="#">11325343</a>	Not Issued	20	01/05/2006	Input circuit for a memory device, and a memory device and memory system employing the input circuit	KIM, KYU-HYOUN
<a href="#">11339120</a>	Not Issued	95	01/23/2006	OUTPUT DRIVER CAPABLE OF CONTROLLING SLEW RATE OF OUTPUT SIGNAL ACCORDING TO OPERATING FREQUENCY INFORMATION OR CAS LATENCY INFORMATION	KIM, KYU-HYOUN
<a href="#">11430199</a>	Not Issued	25	05/09/2006	Phase locked loop circuit and method of locking a phase	KIM, KYU-HYOUN
<a href="#">11430281</a>	Not Issued	20	05/09/2006	Data input and data output control device and method	KIM, KYU-HYOUN

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